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1	US 20040040006 A1	20040226	14	Design method for integrated circuit having scan function	716/8
2	US 6421818 B1	20020716	80	Efficient top-down characterization method	716/18
3	US 6378123 B1	20020423	81	Method of handling macro components in circuit design synthesis	716/18
4	US 6295636 B1	20010925	82	RTL analysis for improved logic synthesis	716/18
5	US 6292931 B1	20010918	81	RTL analysis tool	716/18
6	US 6289498 B1	20010911	81	VDHL/Verilog expertise and gate synthesis automation system	716/18
7	US 6289491 B1	20010911	80	Netlist analysis tool by degree of conformity	716/5
8	US 6263483 B1	20010717	81	Method of accessing the generic netlist created by synopsys design compiler	716/18
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10	US 6173435 B1	20010109	80	Internal clock handling in synthesis script	716/18